



LOW POWER CLASS AB SI POWER AMPLIFIER FOR WIRELESS MEDICAL SENSOR NETWORK

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ABSTRACT

The objective of this research was to design a 2.4 GHz class AB Power Amplifier (PA), with 0.18um Semiconductor Manufacturing International Corporation (SMIC) CMOS technology by using Cadence software, for health care applications. The ultimate goal for such application is to minimize the trade-offs between performance and cost, and between performance and low power consumption design. This paper introduces the design of a 2.4GHz class AB power amplifier which consists of two stage amplifiers. This power amplifier can transmit 10dBm output power to a 50Ω load. The power added efficiency is 7.5% at 1dB compression point and the power gain is 10dB, the total power consumption is 0.135W. The performance of the power amplifier meets the specification requirements of the desired.

KEYWORDS

Two stage, Class AB, Power amplifier, Healthcare

1. INTRODUCTION

Wireless Sensor Networks (WSN) can be widely applied to solve a vast array of problems, under varied conditions [1]. By spatially distributing many devices to monitor the surrounding environment, WSNs can provide continuous, near-real time data over a large sampling area or population [2][3]. WSNs can provide considerable efficiencies to otherwise costly tasks. For example, outpatient monitoring carries considerable cost, especially if applied to a large segment of the patient population. Cost-effective solutions can be established leveraging WSNs and the existing cellular communication infrastructure. Academic and hospital research is currently ongoing investigating such frameworks [4][5][6][7][8].

Due to current hardware limitations, healthcare application of WSNs are still in the early stages [9]. Such devices require Food and Drug Administration (FDA) approval, which can be challenging and costly due to the requirement that the devices pass a number of safety tests. This has been historically challenging, with only a limited number of companies successfully building and fielding a device under full FDA approval [10].

WSNs consist of a number of networked elements, which are individually called sensor nodes. Sensor nodes contain a number of common hardware elements such as microprocessors, memory, batteries, MEMS sensors, antennas, etc. A major design constraint for medical applications is that - since it is a consumer application - designs must meet functional requirements while being cost-effective. In order to implement networks with a large number of



nodes (for example with one node per patient), each node must be low cost. For many applications, WSN nodes have challenging power requirements, as well. Typically, each node must offer long working cycles without battery recharging. This drives most sensor node designs to be ultra-low power devices. Achieving this low power performance at low cost are critical to making such sensor networks feasible.

In this pursuit, designs can reduce costs by leveraging the rapid development and widespread use of wireless systems. The wireless hardware industry, driven by global consumer demand, already strives for low cost, compact designs with flexible functionality. Transceivers systems are typically implemented in the Complementary Metal-Oxide Semiconductor (CMOS) technology. CMOS is a highly matured and well-understood technology. Advanced CMOS technologies can integrate the digital, analog and Radio Frequency (RF) components on a single, tiny chip.

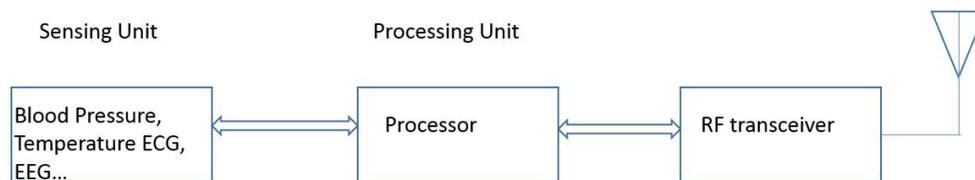


Figure 1. Block diagram of a typical sensor node

Figure 1 shows that the basic sensing node can collect the physiological signals (e.g.: such as EEG, ECG, body temperature, blood pressure, heart beat etc.), when attached to a human body [9]. The processing unit processes all the sensed signals, then sends out the data based on communication protocols. All the processed data will be transmitted through a wireless link to a portable, personal base-station. Doctors can then obtain all the patients' data through the network.

The main challenge for such sensor node is the high power consumption of portable devices. A solution to this challenge is the integration of the portable devices' digital and RF circuitry into one chip.

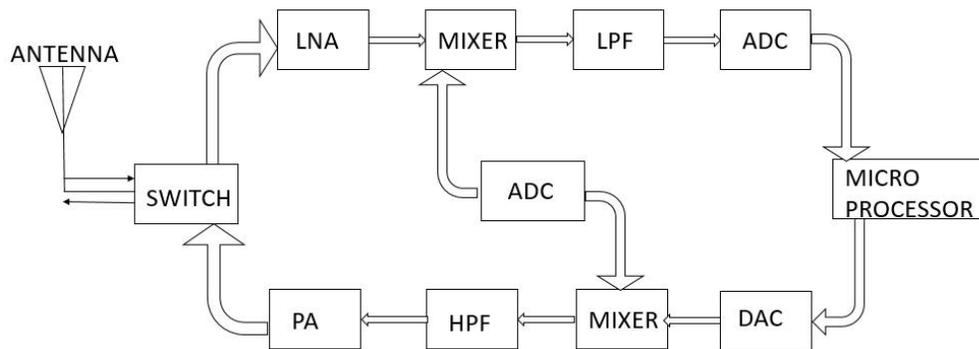


Figure 2. Block diagram of a transmitter

The receiver will receive the signal and will also perform DSP processing after the data is sent out by the transmitter [10]. Figure 2 is the transmitter diagram. It is desirable that the transmitter and receiver are low power devices. The direct-conversion transmitter is very popular for such applications, because it offers versatility, flexibility, spectral efficiency, and low complexity.



These features make the transmitter simpler than the super-heterodyne transmitter. Small chip and circuit size, and low power consumption can be achieved with a direct-conversion transmitter architecture. For the front-end transmitter, the major objectives are 1) transmit RF signals and 2) recover the biosignal classification. This paper proposes a low power receiver design. This paper is mainly for the power amplifier design, since other portions of the circuit design are already discussed in the paper [13]. In order to meet the standards, the PA is designed as shown in table 1.

Table 1: PA design requirement.

Parameter	Target(Unit)
Gain	10dBm
PAE	10%
Stability	>1
S11	-10 dB

2. BACKGROUND INTRODUCTION

Wireless Local Area Networks (WLANs) are everywhere in our daily life, like air or water. During the last 40 years, companies have been busy with implemented WLAN infrastructures into offices to provide more convenience and better data communication across their LAN. For the sake of the interoperability, most WLAN infrastructure use WLAN standards is 802.11a and primarily 802.11b. The 802.11 standard is used to provide solutions for business, home, and “hot spot” WLAN needs [11].

The 802.11b standard was an expansion of the IEEE 802.11 standard. 802.11b can support bandwidths up to 11 Mbps and uses the same radio signalling frequency (2.4 GHz) as 802.11. However, interference can incur from appliances such as microwaves and cordless phones that the same 2.4 GHz range [11]. The pros of the 802.11b standard are lower costs and improved signal range. The cons are slower maximum speed fewer simultaneous users, and appliances can interfere with the frequency band.

The 802.11a standard is another extension of the original 802.11 standard. What many people do not know is that 802.11a was created at the same time as 802.11b. This is due to the fact that 802.11b is more popular than the 802.11a. While 802.11b targets the home market, 802.11a standard is more suitable for the business market because of its higher cost. The pros of the 802.11a are faster speeds to support more users at the same time and the use of specific frequencies which can prevent devices from interfering with each other. The cons are higher cost, a shorter range than 802.11b, and that it can be easily blocked.

A new standard is 802.11g, which also has a speed of 54Mbps, similar to 802.11a. It is important to note that 802.11g is more attractive because it operates in the lower 2.4GHz unlicensed radio band, while 802.11a operates in the higher 5GHz unlicensed radio band. In other words, compared to 802.11a, 802.11g throughput drops slower over distance [12]. On the other hand, sometimes the 802.11a standard is preferred, because the 5GHz band provides many more channels than 802.11g [11].

With an 802.11g access point, 802.11b and 802.11g network interface cards (NICs) can operate together. This makes transition 802.11g smooth for existing 802.11b networks because NICs can still work with the newer 802.11g access points [12].



Bluetooth is another wireless technology that has a different purposes comparable to WLAN [5]. It is designed to functioning in personal area networks (PANs) where a few devices are carried by a person around their desk. The pros of bluetooth are its lower cost, lower battery consumption, and the fact that it provides application profiles, which are application-layer standards that are designed to allow users to work together spontaneously, with little intercession [12].

In contrast, the cons associated with bluetooth include its rated speed, distance, number of devices, and scalability. Bluetooth provides 722 kbps with a back channel of 56 kbps which it may increase. However, it is much slower than 802.11 standards. Also, its maximum coverage is only 10 meters. Bluetooth scalability is poor compared to 802.11, because 802.11 has more multiple access points [12].

The problem that bluetooth has is that it can interfere with 802.11b networks because they both operate in the 2.4GHz band. People are currently working to reduce transmission interference between these two networks but they still have some problems [14].

Many communication standards are widely used in our current daily life in applications, such as cellular networks, personal area networks (PAN), wireless local area networks (WLAN), and the upcoming wireless metropolitan area networks (WiMAX). These wireless standards include Bluetooth, IEEE802.1x, and Zigbee, and are suitable for covering short distances at a low cost. Using a receiver and transmitter in one Si chip is more reasonable for maintaining low costs. Insufficient power consumption is another concern for wireless devices implementing these standards. The device's low power can be achieved by the specific architecture, but this can reduce its flexibility. Additionally, due to the limited available bandwidth of the FCC, new standards for higher data rates will require the use of non-constant envelope modulation techniques which introduce even great power consumption by the device [10].

3. METHODS

Over the past 30 years, research on CMOS radio-frequency (RF) front-end circuits has progressed extremely quickly. The ultimate goal for the wireless industry is to minimize the trade-offs between performance and cost, and between performance and low power consumption design [15].

The proposed Class AB amplifier has low output power and good linearity based on the IEEE 802.11b communication protocol. The class AB power amplifier topology is shown in figure 3. The 2.4GHz PA is a two stage common-source amplifier. The first stage is a driver stage, used for providing sufficient driving capability and a proper gain, as seen in figure 4(a), and the second stage is the power output stage which used for performing sufficient output power, as seen in figure 4(b) [16].

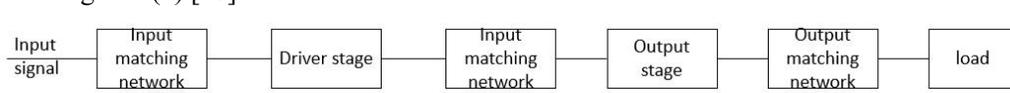


Figure 3. Block diagram of a class AB power amplifier

To ensure low cost, so the PA is designed via a CMOS process. And the initial requirements as seen in Table1.

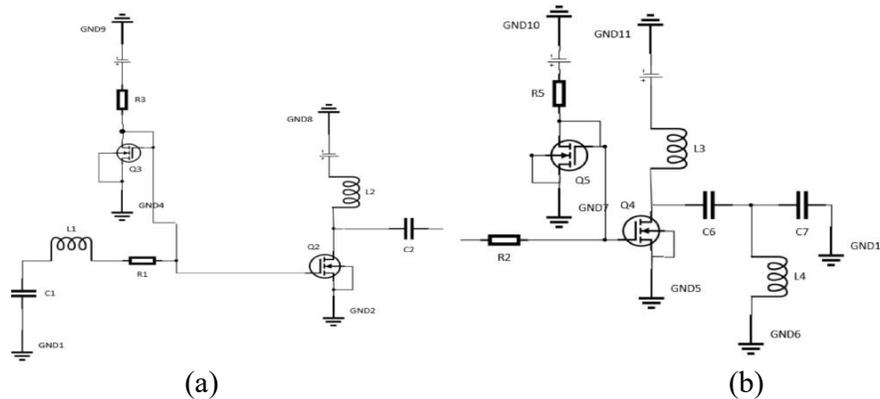


Figure 4. (a) Schematic of driver stage (b) Schematic of output stage

For the drive-level circuit, the first design concern was ensuring the input and output conjugate match to different sizes of CMOS transistor. To get the optimum bias, small-signal simulation and 1dB compression point simulation are completed by their power output capability. Resulting design values can be shown in Table 2 and Table3.

Table 2: 2.4GHz PA driver stage component.

Parameter	Size (Unit)
Q2	W/L=4.8um/1um (f=16,m=12)
Q3	W/L=0.3um/1um
R1	14.5 Ohm
R3	13K Ohm
L1	22 nH(Q=20)
L2	15 nH (Q=20)
C1	200 fF
C2	10 pF

After the output stage and driver stage, the inter-stage matching circuit is more challenging. If the input of second stage and output of the first stage are all conjugate matched to 50 , the two stages can be connected directly. The complete optimized circuit is shown in Figure 5.

Table 3: 2.4GHz PA Output Stage Component.

Parameter	Size (Unit)
Q4	W/L=4.8um/3um (f=16,m=12)
Q5	W/L=0.3um/1.2um
R2	22.2 Ohm
R5	7K Ohm
L3	15 nH(Q=20)
L4	400 nH (Q=20)
C6	800 fF
C7	20 pF

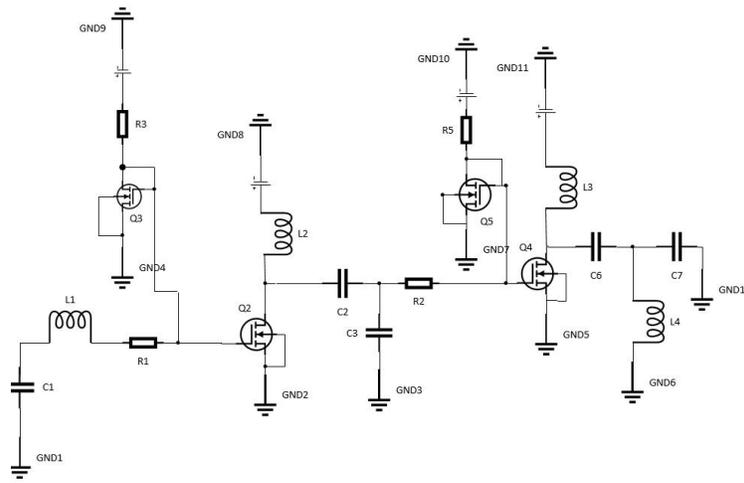


Figure 5. Overall circuit schematic

4. RESULTS

As seen in figure 6(a), the gain is 10. As seen in figure 6(b), the frequency is at 2.4 GHz the S11 is less than -10 dB, also, the total power of the PA is 0.135 W.

As seen in figure 7(a), Kf is larger than 1 for all frequencies from 1 to 3 GHz, so this circuit is totally stable. And the PAE is 7.5%.

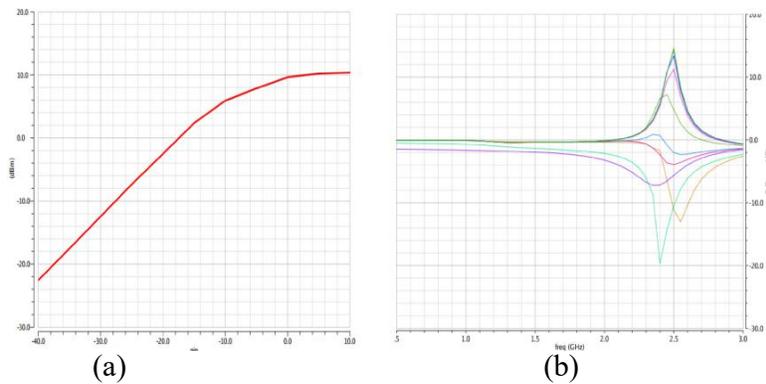


Figure 6. (a) Output power (b) S11

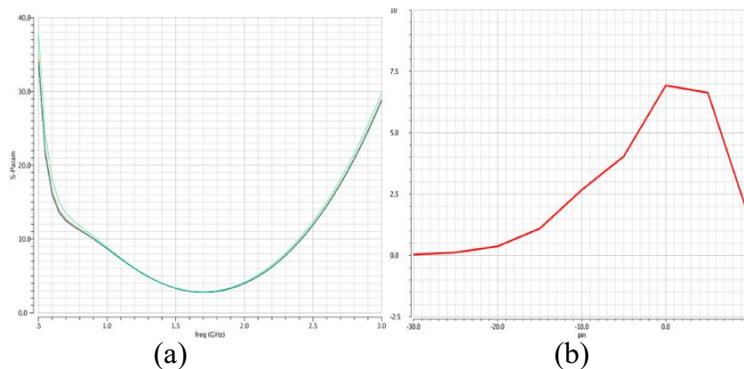


Figure 7. (a) Kf (b) PAE



5. CONCLUSION

This paper describes the method of designing and simulating power amplifier using cadence software based on SIMC CMOS process 180nm technology. This PA is used for sensor networks. This research is still in the early stages of development of a low cost and low power device. In order to reach the performance that is needed, the PA process uses group III and IV elements. This circuit meets the scheduled requirements for the CMOS process, but it still has room to improve performance metrics. When the sensor is coupled with communications technologies such as mobile phones and the Internet, the sensor network constant information flow between individuals and their doctors. Such low cost and low power device can save a lot of hospitalization resources. To realize this, future improvement is needed.

6. FUTURE WORK

This technologies are extremely important, because they can detect and prevent illness without a patient ever leaving their home. Thus, they could reduce hospital readmission rates, save hospital resources and save patients money. Remote monitoring systems help patients be aware of their physical conditions, and communicate more efficiently with their physicians.

In order to build a complete transceiver, PA block is not enough, as seen in the figure 2, and more blockers should be done [13]. Also, more work can be done to improve the performance, such as better PA topology. I can cover and explore more deeply on this topic if time permitted. I believe power consumption is very important for healthcare applications. In order to achieve an ultra- low power system, system and circuit design both need improvements.

Secondly, since the technology nodes are becoming smaller and smaller, technology creates more challenges for analog/RF designers. For low supply voltage, it is not easy to design a very linear mixer. Besides, accurate device modelling is needed, due to the leakage and process variations.

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